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U.S. UTILITY Patent Application

PATENT NUMBER and  
ISSUE DATE

APPL NUM 10010162	FILING DATE 11/20/2001	CLASS 438	SUBCLASS 400	GAU 2812	EXAMINER ROMAN, A
<b>**APPLICANTS:</b> Hshieh Fwu-luan; So Koon; Amato John; Pratt Brian;					
<b>**CONTINUING DATA VERIFIED:</b> none AR 06/30/03					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> none AR 06/30/03					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		GS 149			
Verified and Acknowledged Examiners's initials		AR 06/30/03			
TITLE : Method of forming narrow trenches in semiconductor substrates					
U.S. DEPT. OF COMM / PAT. & TM-PTO-436L (Rev. 12-94)					

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
Assistant Examiner			
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
			Print Fig.
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		Primary Examiner	
		Applicati n Examiner	
		<b>PREPARED FOR ISSUE</b>	
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